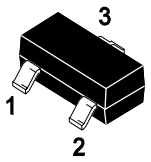
LN4812LT1G

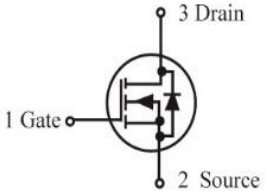
30V N-Channel Enhancement-Mode MOSFET



SOT23(TO-236AB)

1. FEATURES

- VDS= 30V
- We declare that the material of product compliance with RoHS requirements and Halogen Free.



2. APPLICATIONS

- High density cell design for ultra low on-resistance
- Advanced trench process technology
- High power and current handling capability

3. DEVICE MARKING AND ORDERING INFORMATION

Device	Marking	Shipping
LN4812LT1G	N48	3000/Tape&Reel
LN4812LT3G	N48	10000/Tape&Reel

4. MAXIMUM RATINGS(Ta = 25ºC)

Parameter	Symbol	Limits	Unit
Drain–Source Voltage	VDSS	30	V
Gate–to–Source Voltage – Continuous	VGS	±20	V
Drain Current – Continuous TA = 25°C – Pulsed(Note 1)	 ID IDM	 6 30	A

5. THERMAL CHARACTERISTICS

Parameter	Symbol	Limits	Unit
Maximum Power Dissipation	PD	1.4	W
Thermal Resistance, Junction–to–Ambient(Note 2)	RΘJA	90	ºC/W
Thermal Resistance, Junction–to–Ambient(Note 3)	RΘJA	205	ºC/W
Thermal Resistance, Junction–to–Case(Note 2)	RΘJC	75	ºC/W
Operating Junction and Storage temperature Range	TJ,Tstg	−55~+150	° C

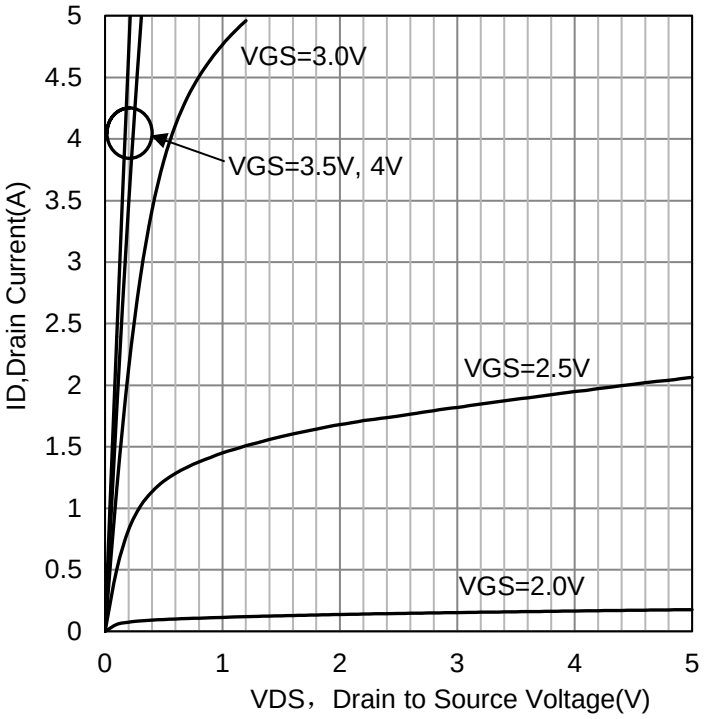
1. Repetitive Rating: Pulse width limited by the Maximum junction temperation.
2. 1-in² 2oz Cu PCB board.
3. Surface−mounted on FR4 board using the minimum recommended pad size.

6. ELECTRICAL CHARACTERISTICS (Ta= 25°C)

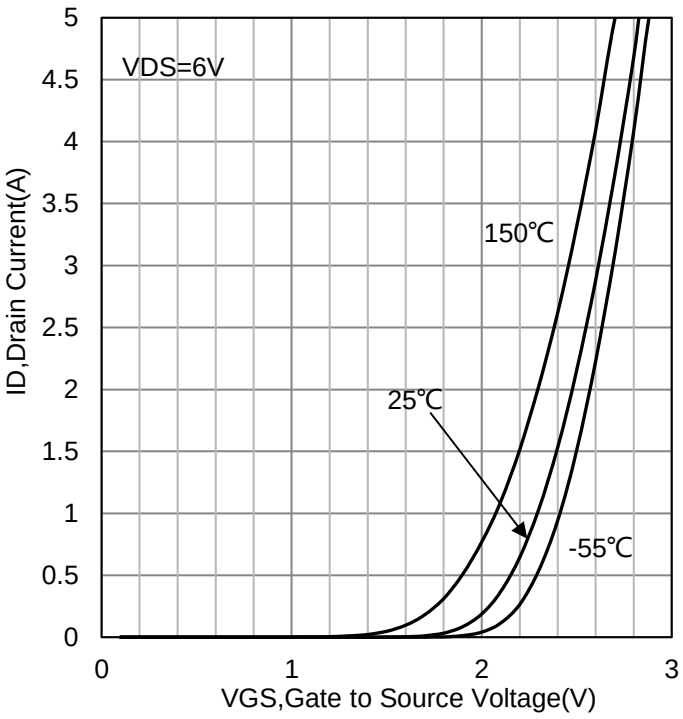
Characteristic		Symbol	Min.	Typ.	Max	Unit
Static						
Drain–Source Breakdown Voltage (VGS = 0, ID = 250μA)		V(BR)DSS	30	-	-	V
Zero Gate Voltage Drain Current (VDS=24V, VGS=0V)		IDSS	-	-	1	μA
Gate–Body Leakage Current, Forward (VDS = 0 V, VGS = 20 V)		IGSSF	-	-	100	nA
Gate–Body Leakage Current, Reverse (VDS = 0 V, VGS = -20 V)		IGSSR	-	-	-100	nA
Gate Threshold Voltage (VDS = VGS, ID = 250μA)		VGS(th)	1.0	1.5	2.1	V
Static Drain–Source On–State Resistance (VGS = 10 V, ID = 6 A) (VGS = 4.5 V, ID = 5 A)		RDS(on)	- -	22 35	38 55	mΩ
Dynamic						
Input Capacitance (VGS = 0 V, f = 1.0MHz,VDS= 15 V)		Ciss	-	610	-	pF
Output Capacitance (VGS = 0 V, f = 1.0MHz,VDS= 15 V)		Coss	-	100	-	pF
Reverse Transfer Capacitance (VGS = 0 V, f = 1.0MHz,VDS= 15 V)		Crss	-	77	-	pF
Turn-On Delay Time	(VDD = 15V, RL =15Ω, ID = 1A, VGEN = 10V RG = 6Ω)	td(on)	-	9	-	ns
Rise Time		tr	-	14	-	
Turn-Off Delay Time		td(off)	-	30	-	
Fall Time		tf	-	5	-	
Forward Voltage (VGS = 0 V, ISD = 1 A)		VSD	-	-	1.3	V
Max.Diode Forward Current		IS	-	-	3	A

3.Pulse Test: Pulse Width ≤300 μs, Duty Cycle ≤2.0%.

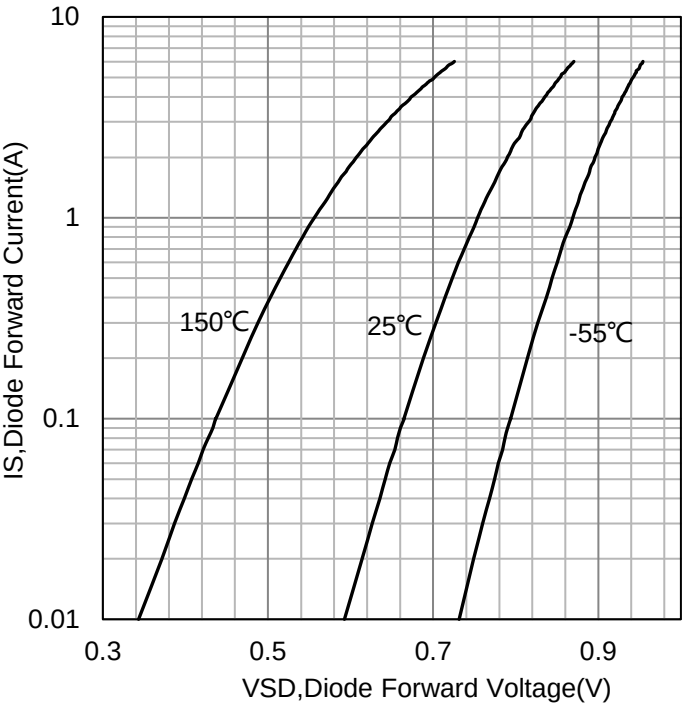
7. ELECTRICAL CHARACTERISTICS CURVES



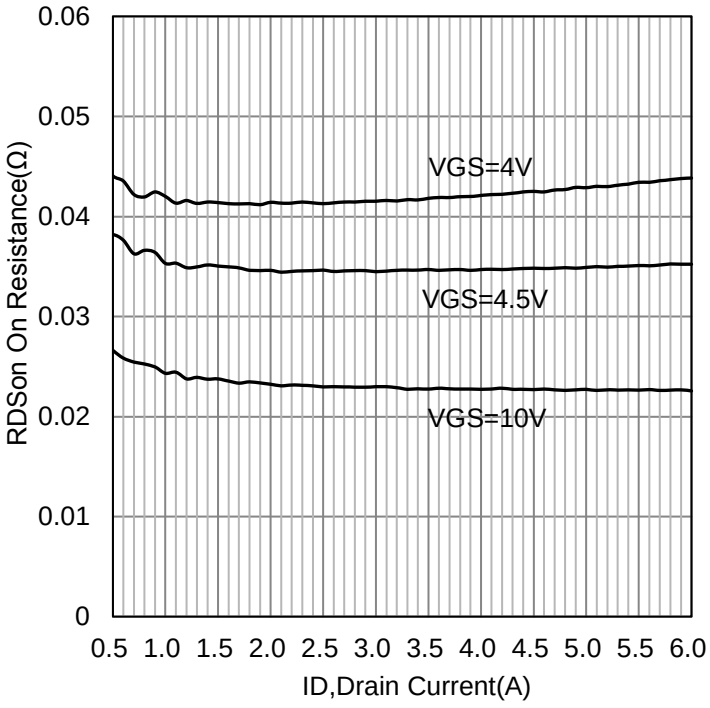
ID vs. VDS



ID vs. VGS

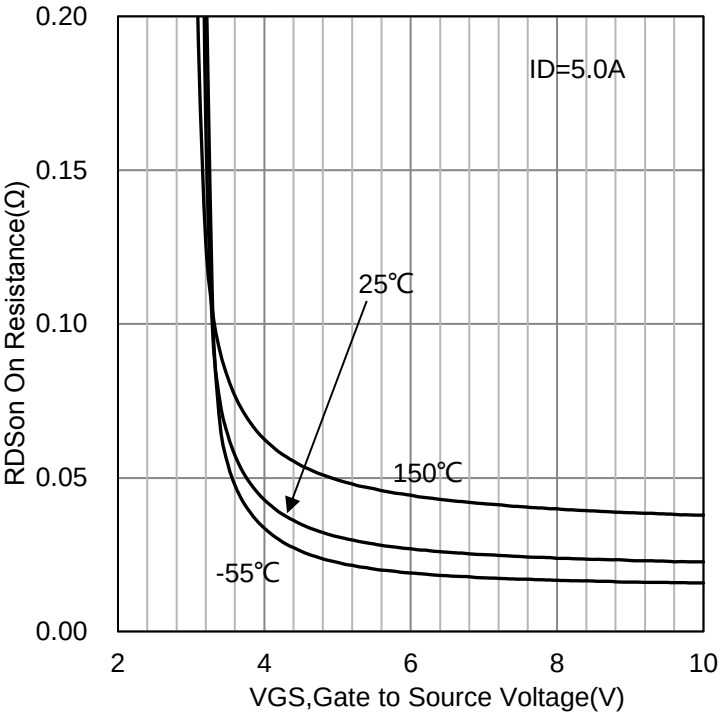


IS vs. VSD

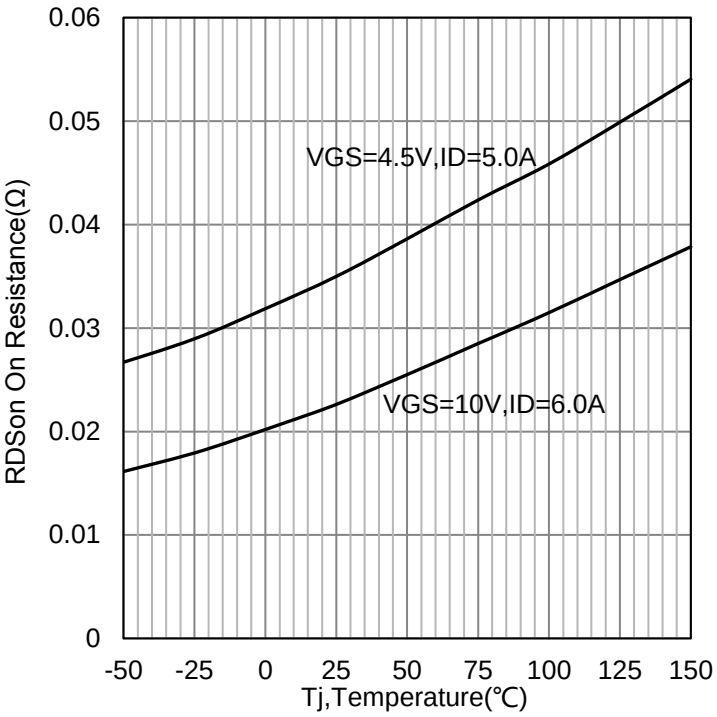


RDS(on) vs. ID

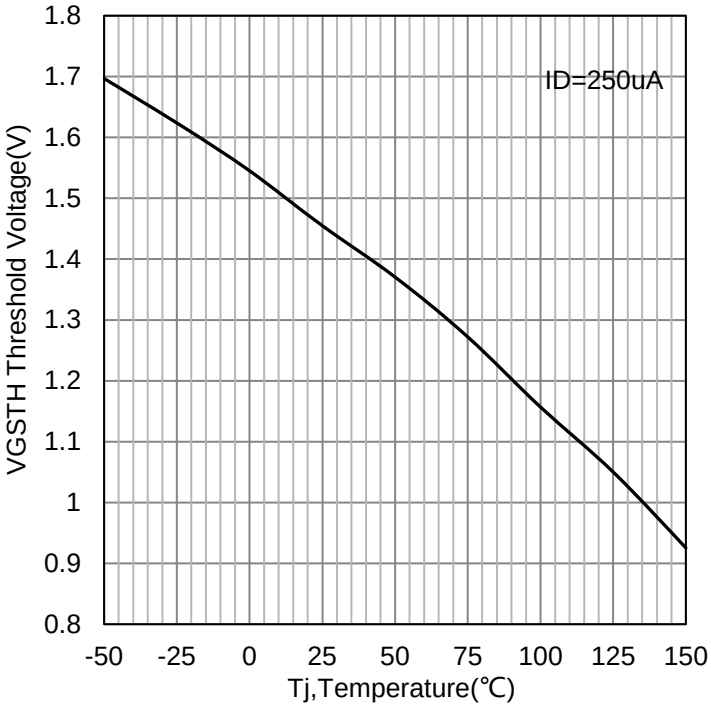
7. ELECTRICAL CHARACTERISTICS CURVES（Con.）



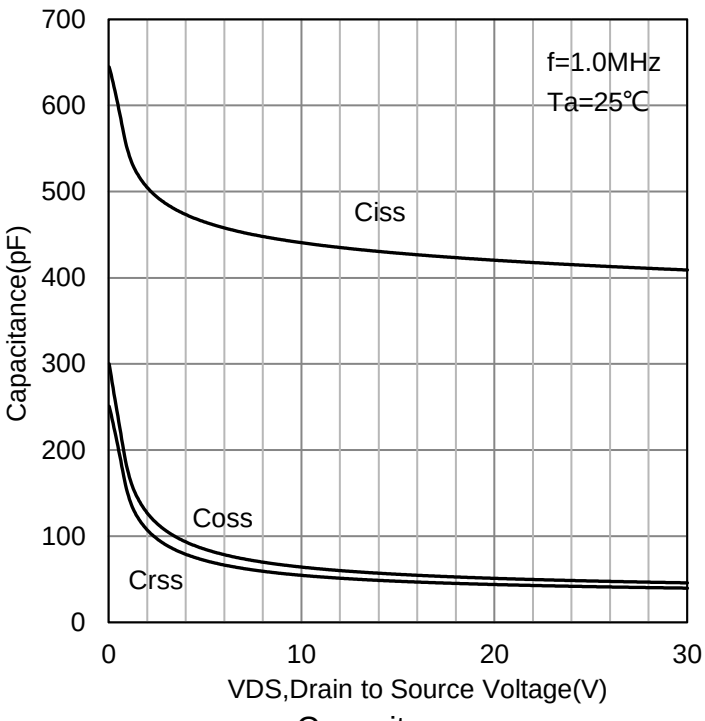
RDS(on) vs. VGS



RDS(on) vs. Tj

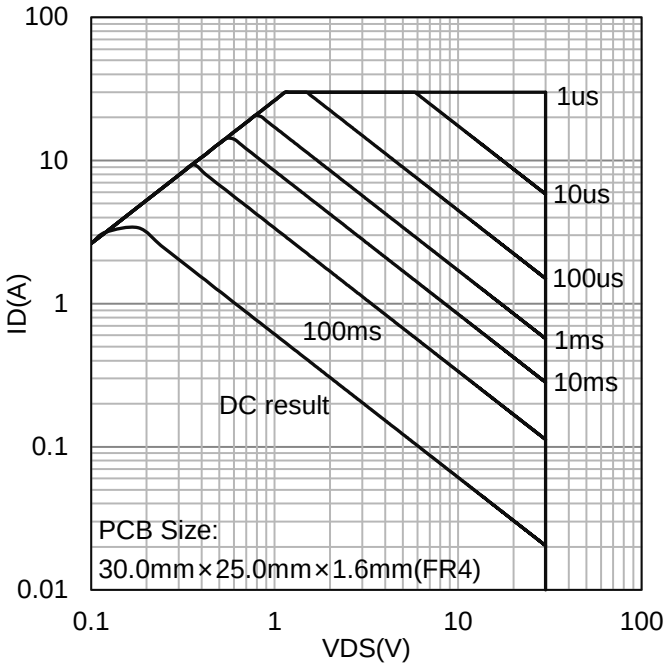


VGSTH vs. Tj



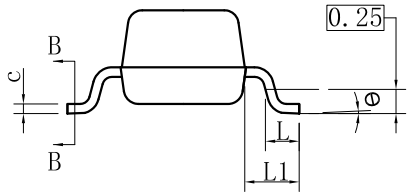
Capacitance

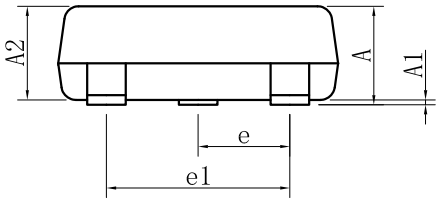
7. ELECTRICAL CHARACTERISTICS CURVES(Con.)

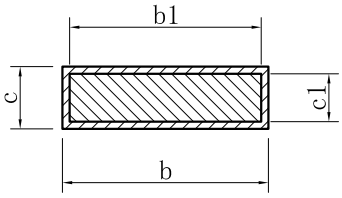


Safe Operating Area

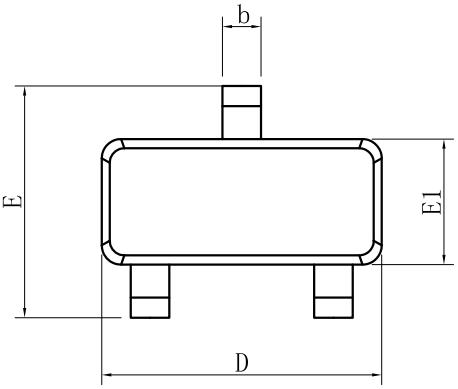
8.OUTLINE AND DIMENSIONS







SECTION B-B

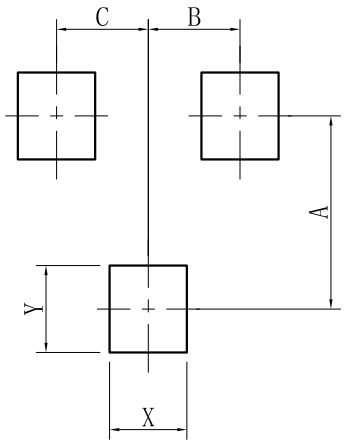


SOT23			
DIM	MIN	NOR	MAX
A	0.89	-	1.12
A1	0.01	-	0.10
A2	0.88	0.95	1.02
b	0.30	-	0.50
b1	0.30	0.40	0.45
c	0.08	-	0.20
c1	0.08	0.10	0.16
D	2.80	2.90	3.04
E	2.10	-	2.64
E1	1.20	1.30	1.40
e	0.95BSC		
e1	1.90BSC		
L	0.40	0.46	0.60
L1	0.54REF		
θ	0°	-	8°
All Dimensions in mm			

GENERAL NOTES

1. Top package surface finish Ra0.4±0.2um
2. Bottom package surface finish Ra0.7±0.2um
3. Side package surface finish Ra0.4±0.2um

9.SOLDERING FOOTPRINT



SOT23	
DIM	(mm)
X	0.80
Y	0.90
A	2.00
B	0.95
C	0.95

DISCLAIMER

- Curve guarantee in the specification. The curve of test items with electric parameter is used as quality guarantee. The curve of test items without electric parameter is used as reference only.

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