

LP2301LT1G

20V P-Channel Enhancement-Mode MOSFET

1. FEATURES

- $V_{DS} = -20V$
- $R_{DS(ON)}, V_{GS@-2.5V}, I_{DS@-2.0A} = 150m\Omega$
- $R_{DS(ON)}, V_{GS@-4.5V}, I_{DS@-2.8A} = 100m\Omega$
- We declare that the material of product compliance with RoHS requirements and Halogen Free.
- Advanced trench process technology
- High density cell design for ultra low on-resistance
- Fully characterized avalanche voltage and current improved shoot-through FOM

2. APPLICATIONS

- Simple drive requirement
- Small package outline
- Surface mount device

3. DEVICE MARKING AND ORDERING INFORMATION

Device	Marking	Shipping
LP2301LT1G	01	3000/Tape&Reel
LP2301LT3G	01	10000/Tape&Reel

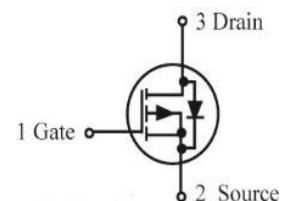
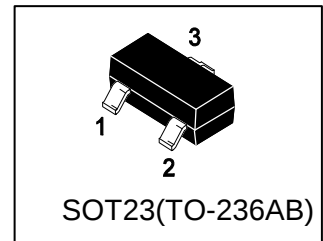
4. MAXIMUM RATINGS($T_a = 25^\circ C$)

Parameter	Symbol	Limits	Unit
Drain-Source Voltage	V_{DSS}	-20	V
Gate-to-Source Voltage – Continuous	V_{GS}	± 8	V
Drain Current			A
– Continuous $T_a = 25^\circ C$	I_D	-2.3	
– Pulsed(Note 1)	I_{DM}	-8	

5. THERMAL CHARACTERISTICS

Parameter	Symbol	Limits	Unit
Maximum Power Dissipation	PD	0.9	W
Thermal Resistance, Junction-to-Ambient(Note 2)	$R_{\theta JA}$	140	$^\circ C/W$
Junction and Storage temperature	T_J, T_{stg}	$-55 \sim +150$	$^\circ C$

1. Repetitive Rating: Pulse width limited by the Maximum junction temperature.
2. 1-in² 2oz Cu PCB board.

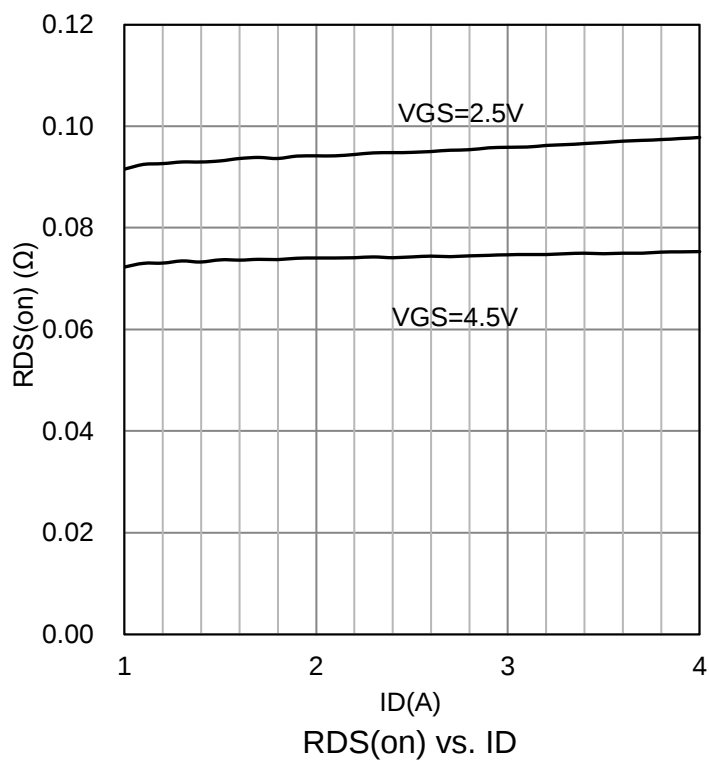
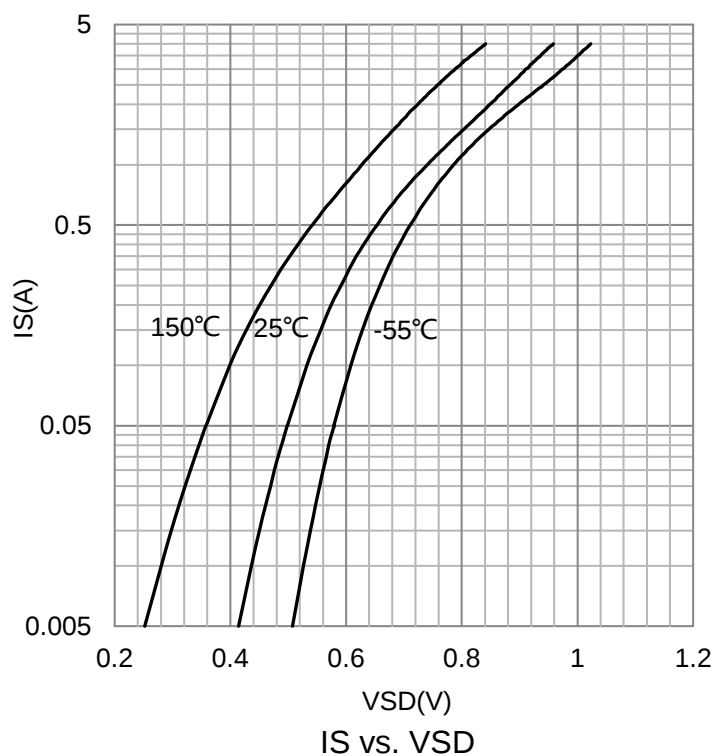
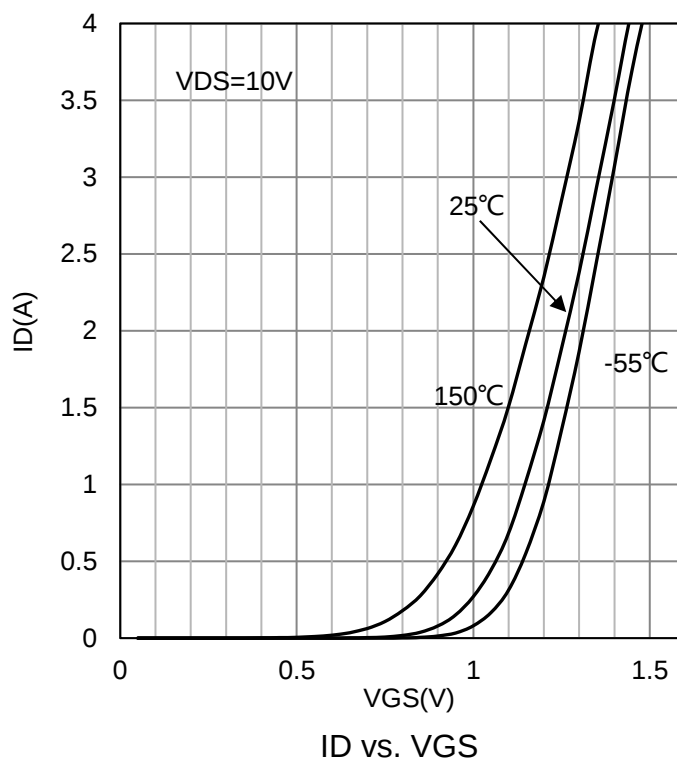
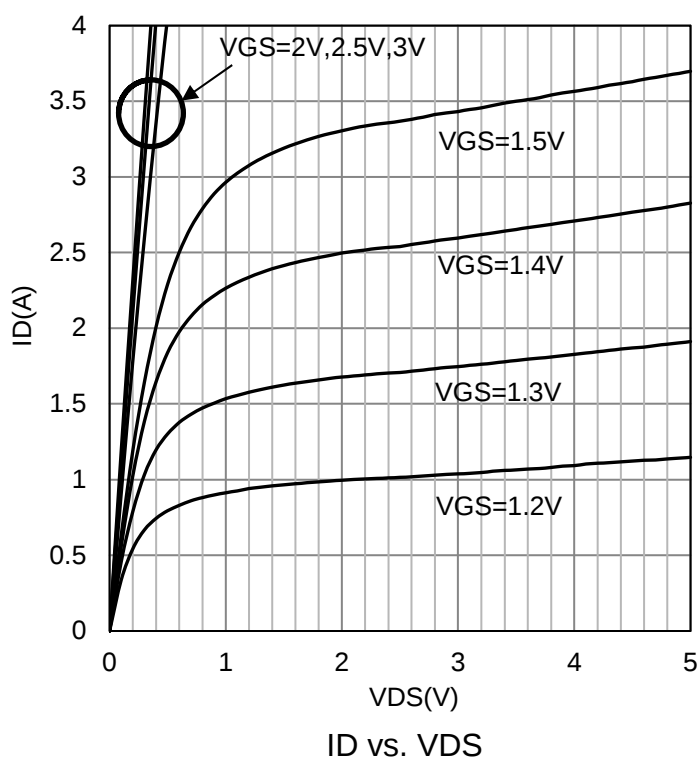


6. ELECTRICAL CHARACTERISTICS (Ta= 25°C)

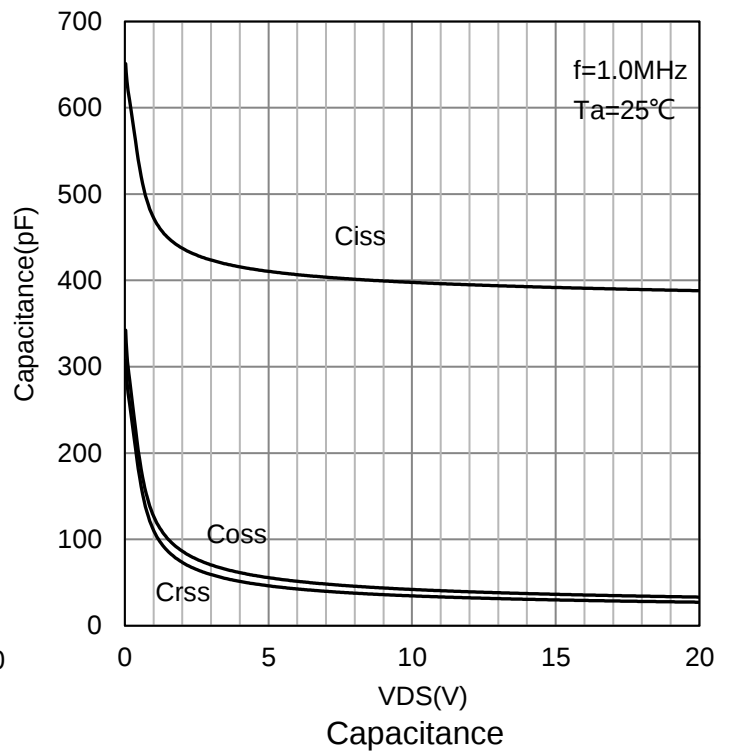
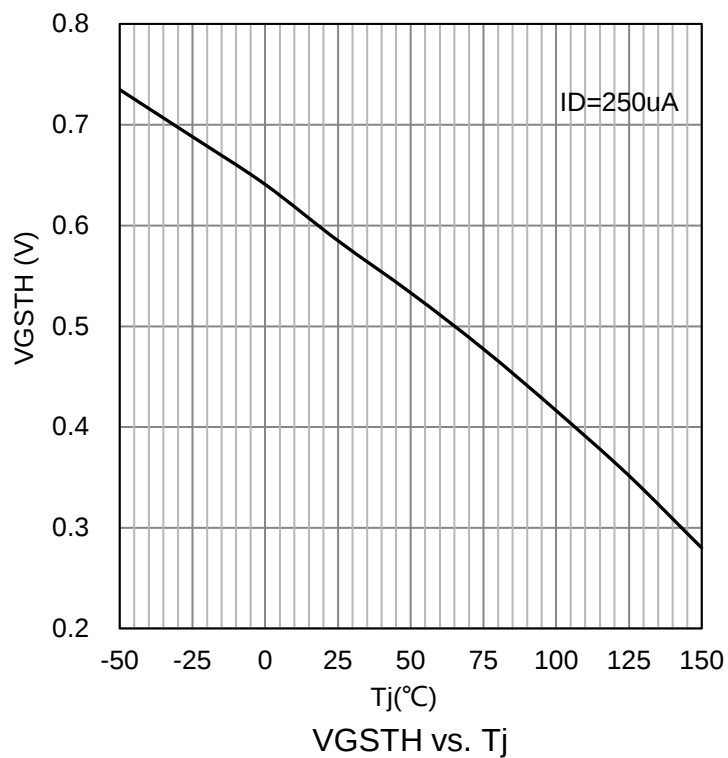
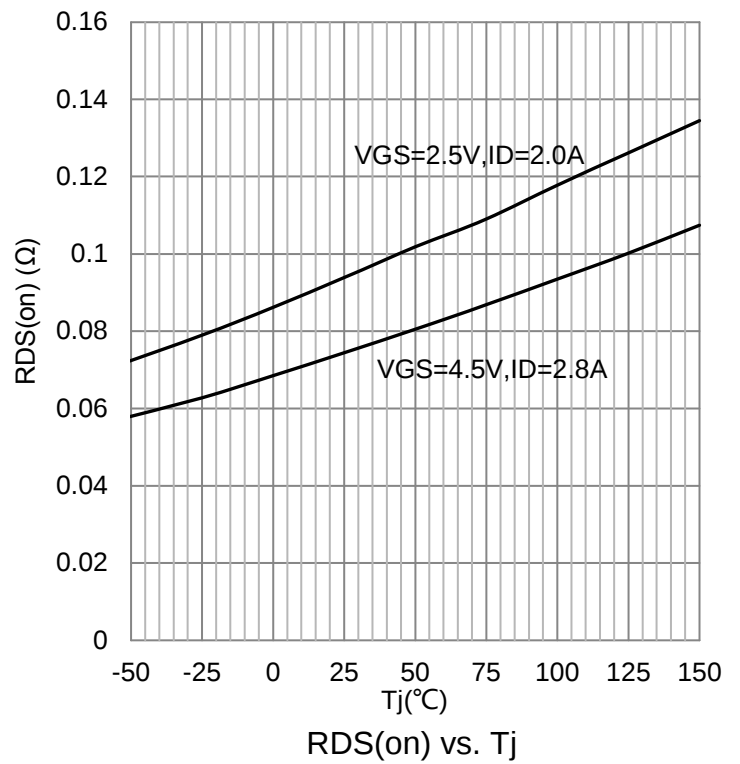
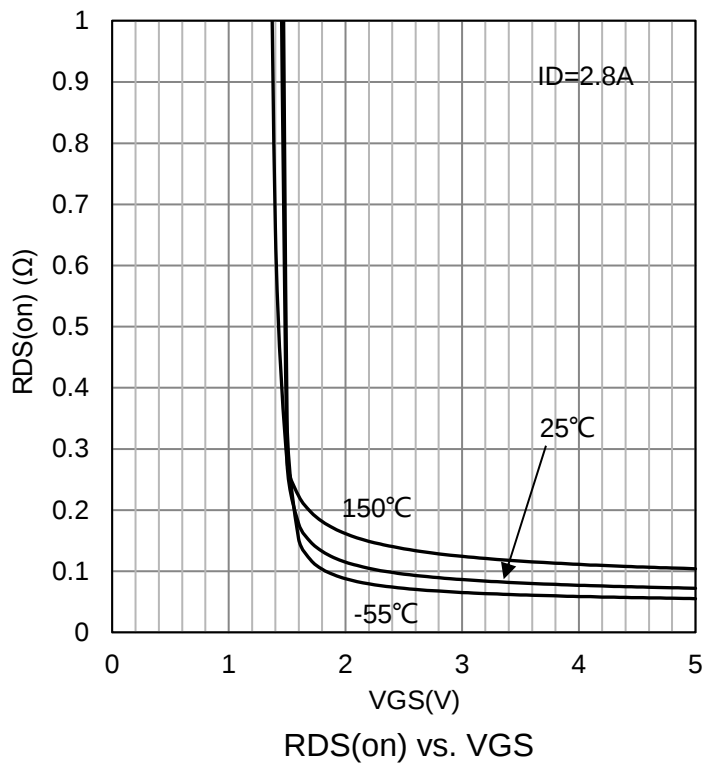
Characteristic	Symbol	Min.	Typ.	Max.	Unit
Static					
Drain–Source Breakdown Voltage (VGS = 0V, ID = -250 μ A)	VBRDSS	-20	-	-	V
Zero Gate Voltage Drain Current (VGS = 0V, VDS = -20 V)	IDSS	-	-	-1	μ A
Gate–Body Leakage Current, Forward (VGS = 8 V)	IGSSF	-	-	100	nA
Gate–Body Leakage Current, Reverse (VGS = - 8 V)	IGSSR	-	-	-100	nA
Gate Threshold Voltage (VDS = VGS, ID = -250 μ A)	VGS(th)	-0.4	-	-0.9	V
Static Drain–Source On–State Resistance (VGS = -4.5 V, ID = -2.8 A) (VGS = -2.5 V, ID = -2 A)	RDS(on)	- -	69 83	100 150	m Ω
Dynamic					
Total Gate Charge	(VDS = -10 V, VGS = -4.5 V, ID = -2 A)	Qg	-	6	nC
Gate–Source Charge		Qgs	-	0.8	
Gate–Drain Charge		Qgd	-	1.6	
Input Capacitance (VGS = 0 V, f = 1.0MHz, VDS= -6 V)	Ciss	-	514	-	pF
Output Capacitance (VGS = 0 V, f = 1.0MHz, VDS= -6 V)	Coss	-	68	-	pF
Reverse Transfer Capacitance (VGS = 0 V, f = 1.0MHz, VDS= -6 V)	Crss	-	59	-	pF
Turn-On Delay Time	(VDD = -6 V, RL = 6 Ω ID = -1 A, VGEN = -4.5 V RG = 6 Ω)	td(on)	-	4	ns
Rise Time		tr	-	5	
Turn-Off Delay Time		td(off)	-	91	
Fall Time		tf	-	43	
Forward Voltage (VGS = 0 V, ISD = -0.75 A)	VSD	-	-0.8	-1.2	V

3. Pulse Test: Pulse Width $\leq 300 \mu$ s, Duty Cycle $\leq 2.0\%$.

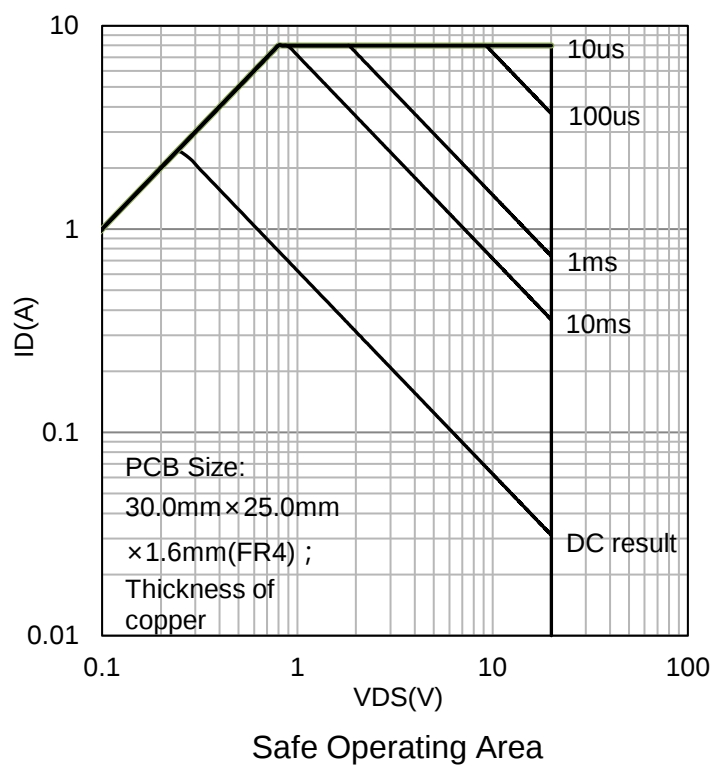
7. ELECTRICAL CHARACTERISTICS CURVES



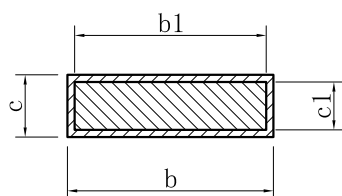
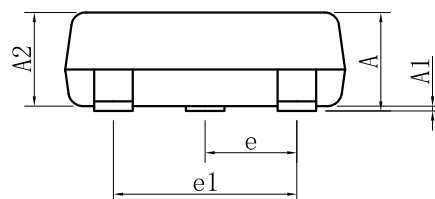
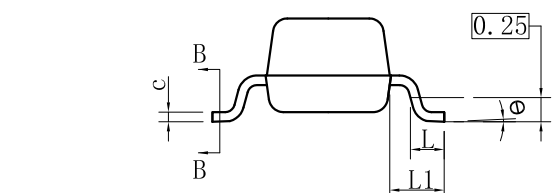
7. ELECTRICAL CHARACTERISTICS CURVES(Con.)



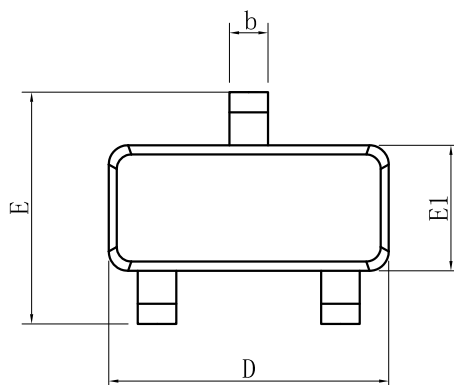
7. ELECTRICAL CHARACTERISTICS CURVES(Con.)



8.OUTLINE AND DIMENSIONS



SECTION B-B

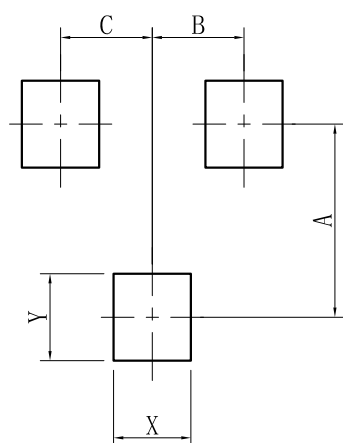


SOT23			
DIM	MIN	NOR	MAX
A	0.89	—	1.12
A1	0.01	—	0.10
A2	0.88	0.95	1.02
b	0.30	—	0.50
b1	0.30	0.40	0.45
c	0.08	—	0.20
c1	0.08	0.10	0.16
D	2.80	2.90	3.04
E	2.10	—	2.64
E1	1.20	1.30	1.40
e	0.95BSC		
e1	1.90BSC		
L	0.40	0.46	0.60
L1	0.54REF		
θ	0°	—	8°
All Dimensions in mm			

GENERAL NOTES

- 1.Top package surface finish $Ra0.4\pm0.2\mu m$
- 2.Bottom package surface finish $Ra0.7\pm0.2\mu m$
- 3.Side package surface finish $Ra0.4\pm0.2\mu m$

9.SOLDERING FOOTPRINT



SOT23	
DIM	(mm)
X	0.80
Y	0.90
A	2.00
B	0.95
C	0.95

DISCLAIMER

- Curve guarantee in the specification. The curve of test items with electric parameter is used as quality guarantee. The curve of test items without electric parameter is used as reference only.
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