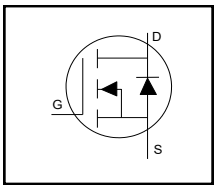
- Logic - Level Gate Drive
- Advanced Process Technology
- Ultra Low On-Resistance
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
- Fully Avalanche Rated
- Lead-Free



V_{DSS}	30V
$R_{DS(on)}$ max.	0.006Ω
I_D	140A⑤

TO-220AB
IRL3803PbF

G	D	S
Gate	Drain	Source

Description

Fifth Generation HEXFETs utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The TO-220 package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 watts. The low thermal resistance and low package cost of the TO-220 contribute to its wide acceptance throughout the industry.

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRL3803PbF	TO-220	Tube	50	IRL3803PbF

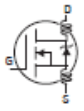
Absolute Maximum Ratings

Symbol	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	140 ⑤	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	98 ⑤	
I_{DM}	Pulsed Drain Current ①	470	
P_D @T_C = 25°C	Maximum Power Dissipation	200	W
	Linear Derating Factor	1.3	W/°C
V_{GS}	Gate-to-Source Voltage	± 16	V
E_{AS}	Single Pulse Avalanche Energy ②	610	mJ
I_{AR}	Avalanche Current ①	71	A
E_{AR}	Repetitive Avalanche Energy ①	20	mJ
dv/dt	Peak Diode Recovery dv/dt ③	5.0	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting torque, 6-32 or M3 screw.	10 lbf•in (1.1N•m)	

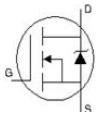
Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	——	0.75	°C/W
$R_{\theta JC}$	Case-to-Sink, Flat, Greased Surface	0.50	——	
$R_{\theta JA}$	Junction-to-Ambient	——	62	

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	30	—	—	V	V_{GS} = 0V, I_D = 250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.052	—	V/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.006	Ω	V_{GS} = 10V, I_D = 71A④
		—	—	0.009		V_{GS} = 4.5V, I_D = 59A ④
$V_{GS(th)}$	Gate Threshold Voltage	1.0	—	—	V	V_{DS} = V_{GS}, I_D = 250µA
gfs	Forward Trans conductance	55	—	—	S	V_{DS} = 25V, I_D = 71A
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	µA	V_{DS} = 30V, V_{GS} = 0V
		—	—	250		V_{DS} = 24V,V_{GS} = 0V,T_J =150°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V_{GS} = 16V
	Gate-to-Source Reverse Leakage	—	—	-100		V_{GS} = -16V
Q_g	Total Gate Charge	—	—	140	nC	I_D = 71A
Q_{gs}	Gate-to-Source Charge	—	—	41		V_{DS} = 24V
Q_{gd}	Gate-to-Drain Charge	—	—	78		V_{GS} = 4.5V , See Fig. 6 and 13④
$t_{d(on)}$	Turn-On Delay Time	—	14	—	ns	V_{DD} = 15V
t_r	Rise Time	—	230	—		I_D = 71A
$t_{d(off)}$	Turn-Off Delay Time	—	29	—		R_G= 1.3Ω
t_f	Fall Time	—	35	—		R_D= 0.2Ω, See Fig. 10④
L_D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact 
L_S	Internal Source Inductance	—	7.5	—		
C_{iss}	Input Capacitance	—	5000	—	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	—	1800	—		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	—	880	—		f = 1.0MHz, See Fig. 5

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	140⑤	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	470		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	T_J = 25°C,I_S = 71A,V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	—	120	180	ns	T_J = 25°C ,I_F = 71A
Q_{rr}	Reverse Recovery Charge	—	450	680	nC	di/dt = 100A/µs ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S +L_D)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig.11)

② V_{DD} = 15V, starting T_J = 25°C, L = 180µH, R_G = 25Ω, I_{AS} = 20A.(See Figure 12)

③ I_{SD} ≤ 71A, di/dt ≤ 130A/µs, V_{DD} ≤ $V_{(BR)DSS}$, T_J ≤ 175°C.

④ Pulse width ≤ 300µs; duty cycle ≤ 2%.

⑤ Calculated continuous current based on maximum allowable junction temperature; for recommended current- handling of the package refer to Design TIP # 93-4

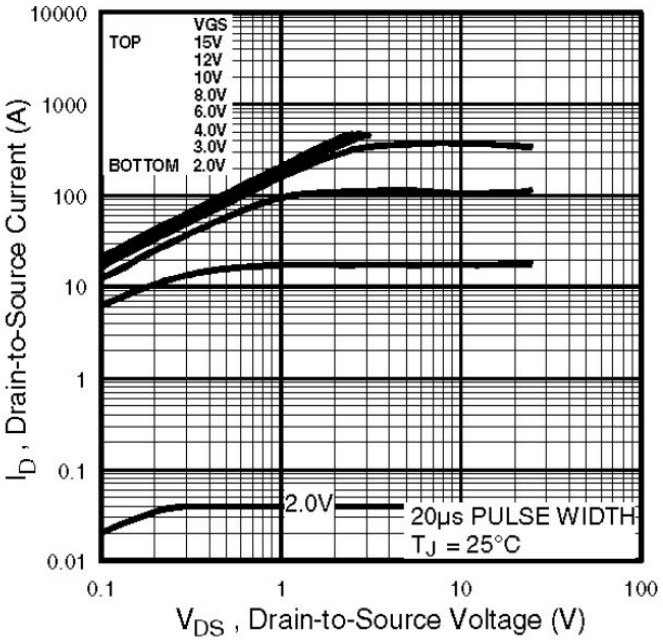


Fig. 1 Typical Output Characteristics
T_J = 25°C

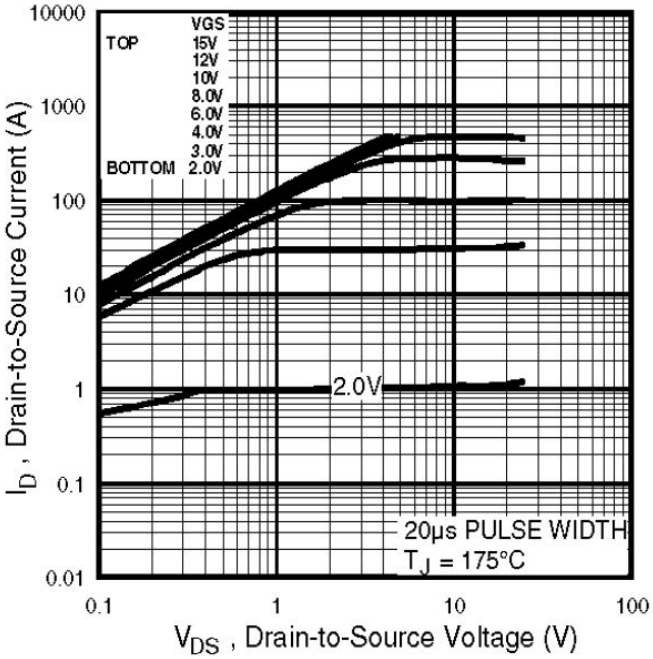


Fig. 2 Typical Output Characteristics
T_J = 175°C

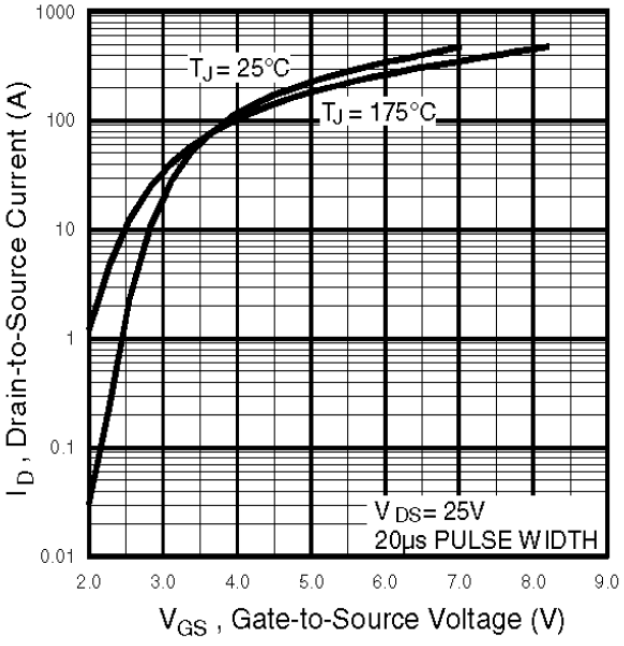


Fig. 3 Typical Transfer Characteristics

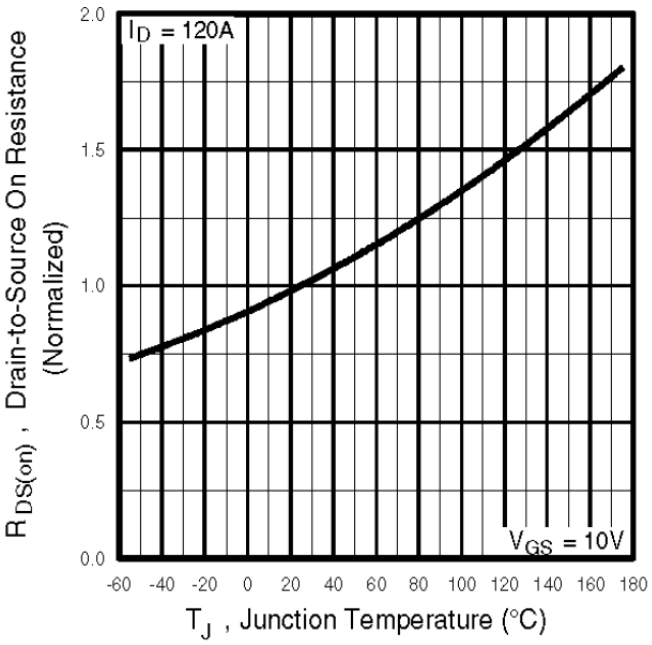


Fig. 4 Normalized On-Resistance vs. Temperature

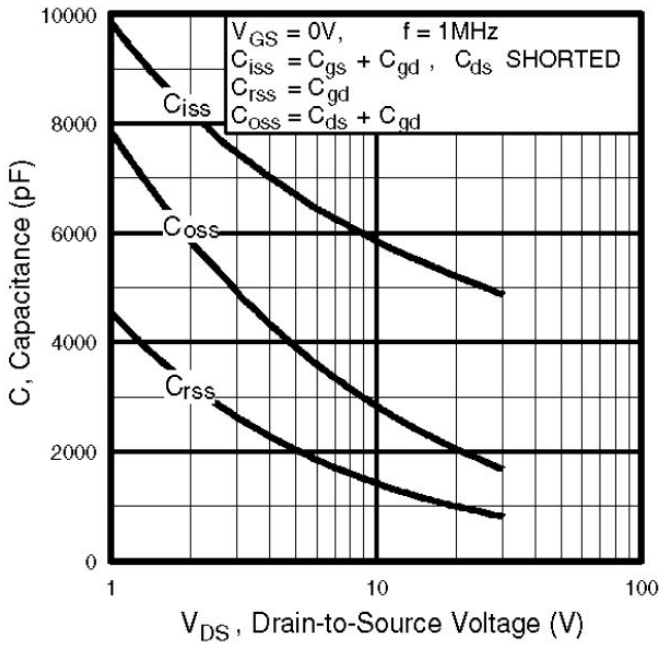


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

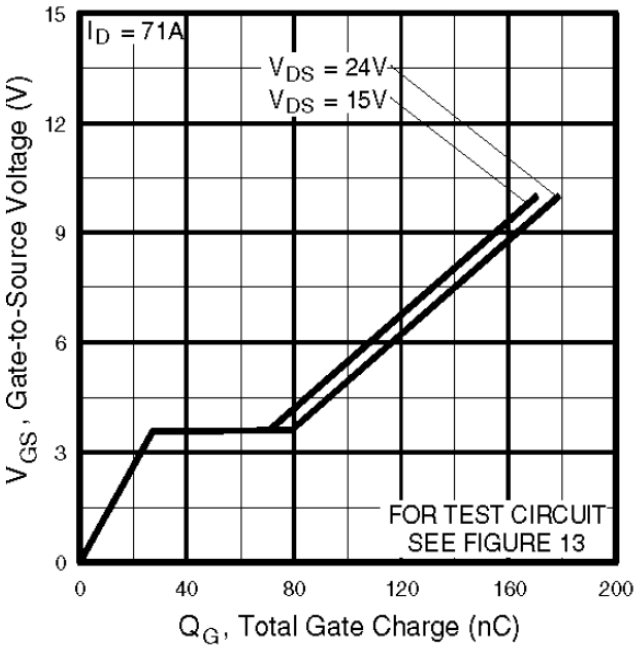


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

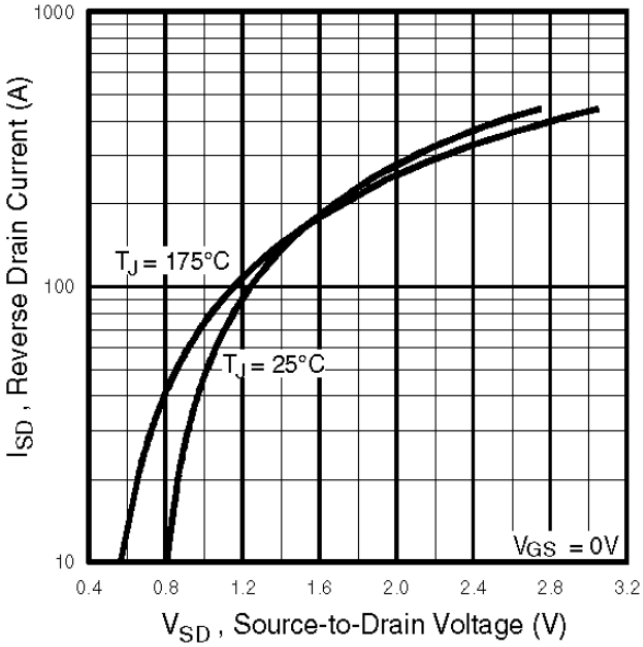


Fig. 7 Typical Source-to-Drain Diode Forward Voltage

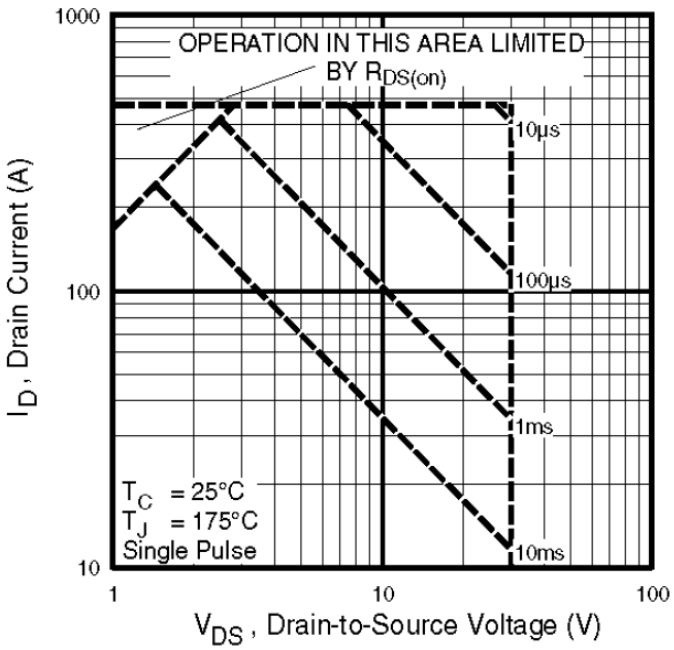


Fig 8. Maximum Safe Operating Area

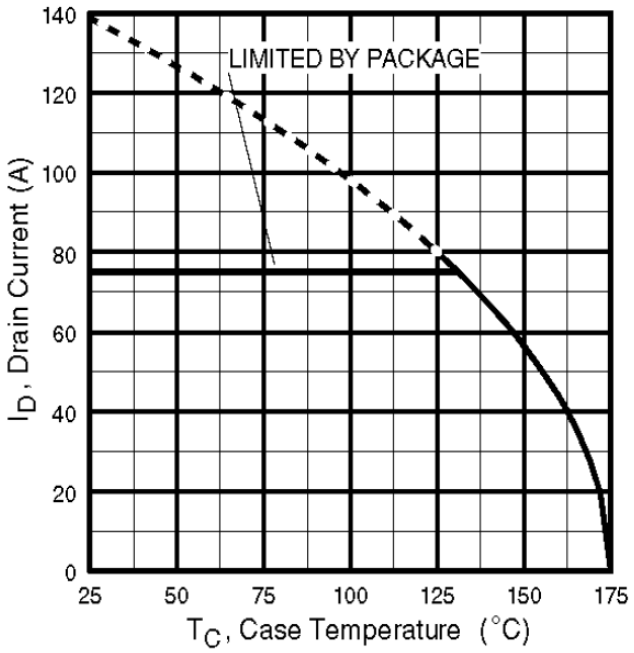


Fig 9. Maximum Drain Current vs. Case Temperature

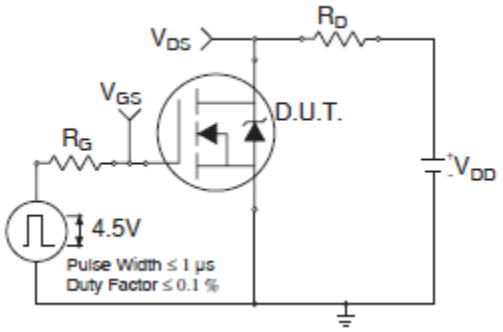


Fig 10a. Switching Time Test Circuit

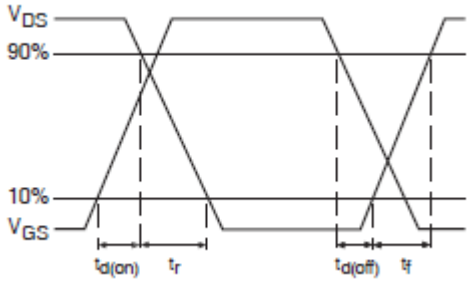


Fig 10b. Switching Time Waveforms

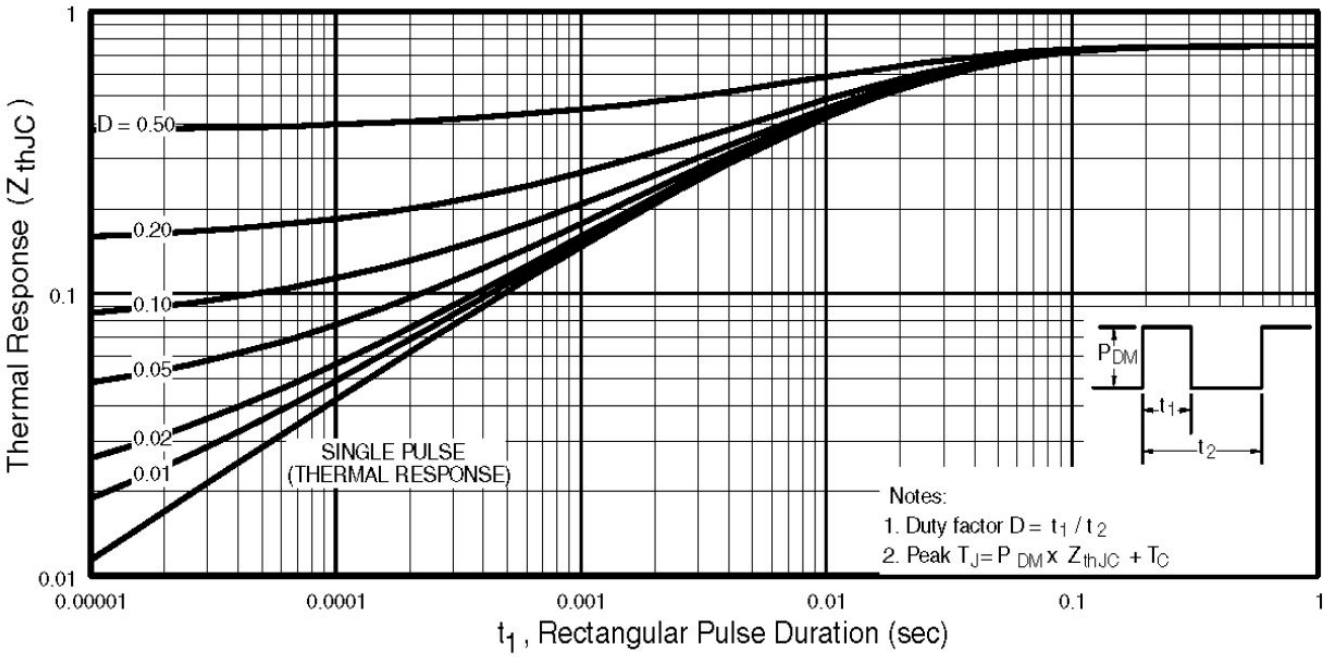


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

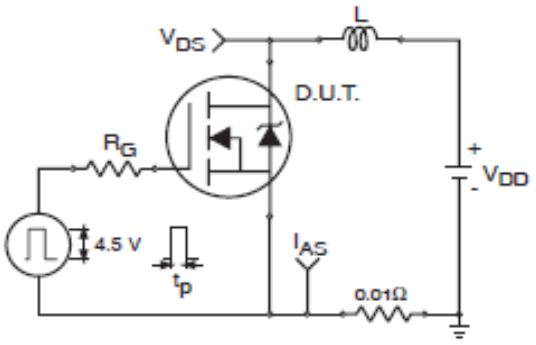


Fig 12a. Unclamped Inductive Test Circuit

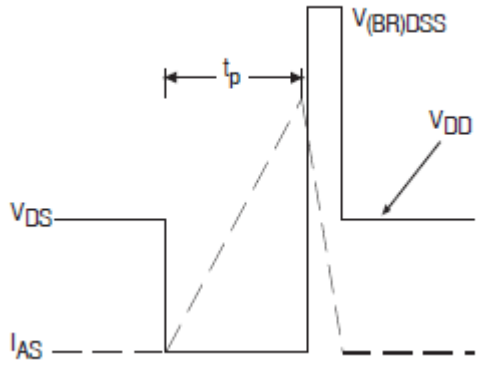


Fig 12b. Unclamped Inductive Waveforms

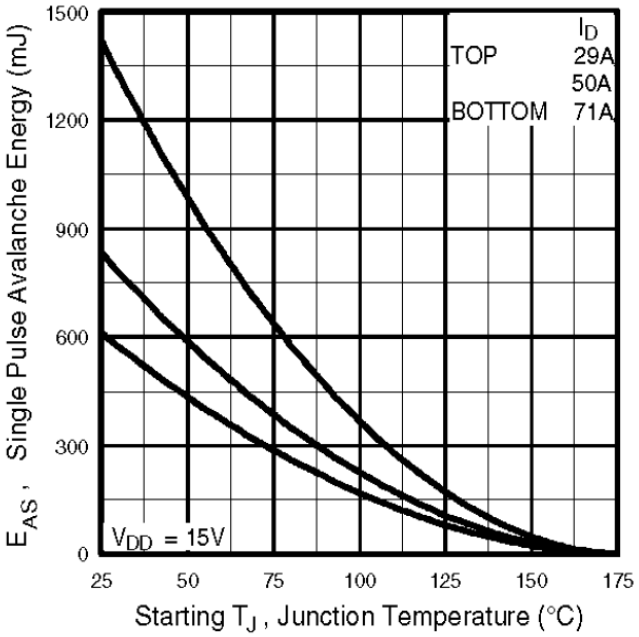


Fig 12c. Maximum Avalanche Energy vs. Drain Current

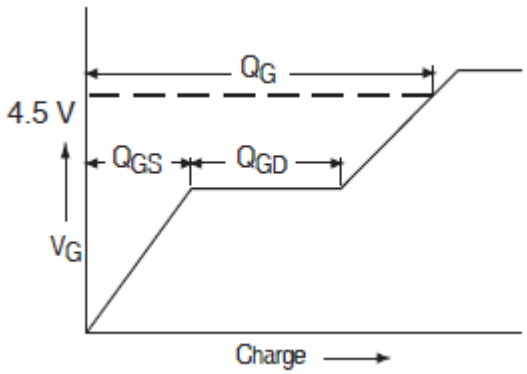


Fig 13a. Gate Charge Waveform

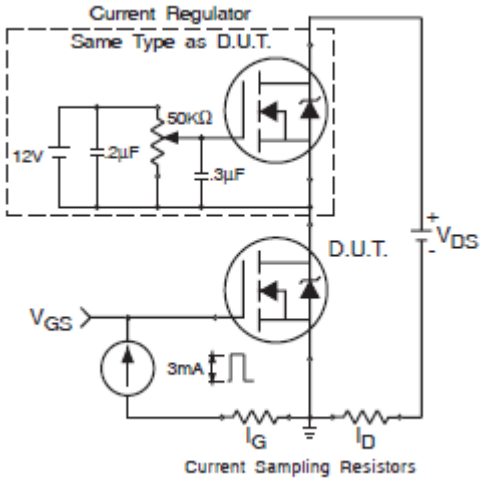
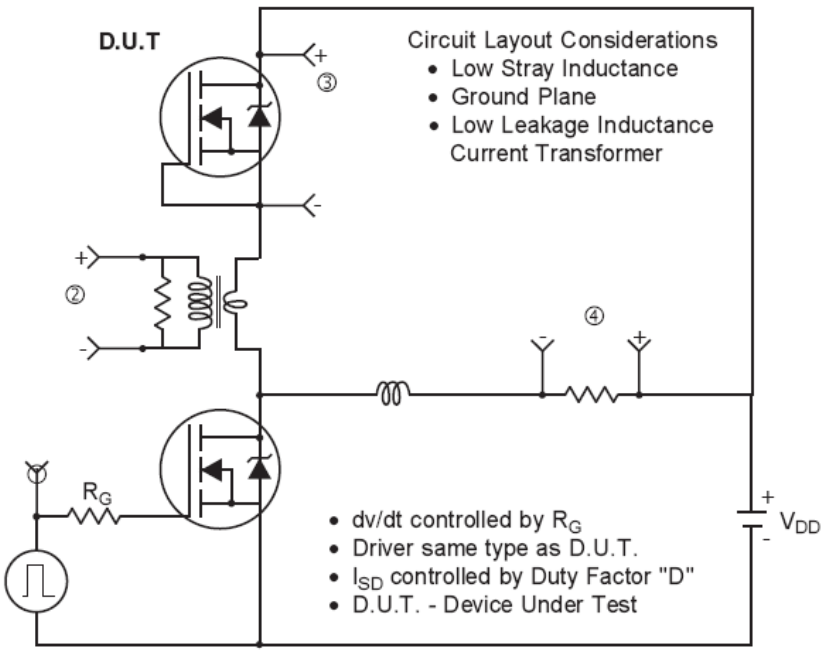


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



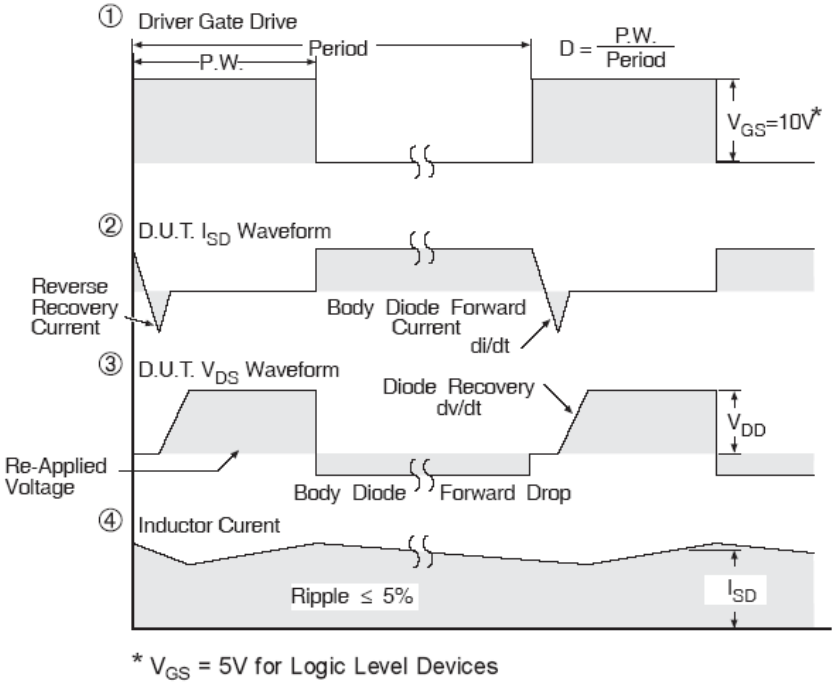
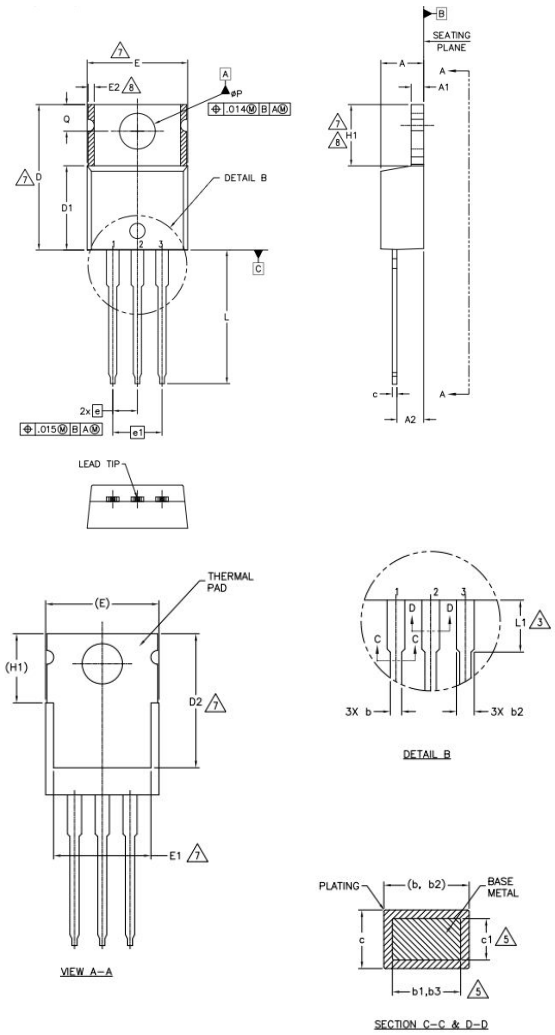


Fig 14. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power

TO-220Package Outline (Dimensions are shown in millimeters (inches)



NOTES:

1.– DIMENSIONING AND TOLERANCING AS PER ASME Y14.5 M– 1994.
2.– DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS].
3.– LEAD DIMENSION AND FINISH UNCONTROLLED IN L1.
4.– DIMENSION D, D1 & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
5.– DIMENSION b1, b3 & c1 APPLY TO BASE METAL ONLY.
6.– CONTROLLING DIMENSION : INCHES.
7.– THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS E,H1,D2 & E1
8.– DIMENSION E2 X H1 DEFINE A ZONE WHERE STAMPING AND SINGULATION IRREGULARITIES ARE ALLOWED.
9.– OUTLINE CONFORMS TO JEDEC TO–220, EXCEPT A2 (max.) AND D2 (min.) WHERE DIMENSIONS ARE DERIVED FROM THE ACTUAL PACKAGE OUTLINE.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	3.56	4.83	.140	.190	
A1	1.14	1.40	.045	.055	
A2	2.03	2.92	.080	.115	
b	0.38	1.01	.015	.040	
b1	0.38	0.97	.015	.038	5
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	5
c	0.36	0.61	.014	.024	
c1	0.36	0.56	.014	.022	5
D	14.22	16.51	.560	.650	4
D1	8.38	9.02	.330	.355	
D2	11.68	12.88	.460	.507	7
E	9.65	10.67	.380	.420	4,7
E1	6.86	8.89	.270	.350	7
E2	–	0.76	–	.030	8
e	2.54 BSC		.100 BSC		
e1	5.08 BSC		.200 BSC		
H1	5.84	6.86	.230	.270	7,8
L	12.70	14.73	.500	.580	
L1	3.56	4.06	.140	.160	3
øP	3.54	4.08	.139	.161	
Q	2.54	3.42	.100	.135	

LEAD ASSIGNMENTS

HEXFET
1.– GATE
2.– DRAIN
3.– SOURCE

IGBTs, CoPACK
1.– GATE
2.– COLLECTOR
3.– EMITTER

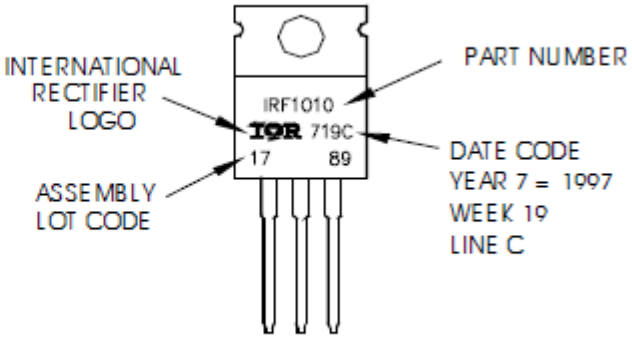
DIODES
1.– ANODE
2.– CATHODE
3.– ANODE

Note: For the most current drawing please refer to website at http://www.irf.com/packaging

TO-220 Part Marking Information

EXAMPLE: THIS IS AN IRF1010
LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE "C"

Note: "P" in assembly line position indicates "Lead-Free"



Note: For the most current drawing please refer to website at http://www.irf.com/packaging

Revision History

Date	Rev.	Comments
02/25/2021	2.1	• Changed datasheet with Infineon logo - all pages. • Updated datasheet based on IFX template. • Removed “HEXFET® Power MOSFET” added “IR MOSFETTM “-page1 • Corrected TO-220 Package outline on page 8. • Added disclaimer on last page.

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Document reference
ifx1